CGD982LC

1 GHz, 23 dB gain GaAs low current power doubler

Rev. 1 — 10 March 2014 Product data sheet

1. Product profile

1.1 General description

Hybrid amplifier module in a SOT115AE package, operating at a supply voltage of 24 V Direct Current (DC), employing Heterojunction Field Effect Transistor (HFET) GaAs dies.

1.2 Features and benefits

- Low power consumption
- Excellent linearity
- Optimized for PAL D loading
- Extremely low noise
- Excellent return loss properties
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)
- Gain compensation over temperature
- Rugged construction
- Unconditionally stable
- Thermally optimized design
- Adjustable supply current

1.3 Applications

- CATV systems operating in the 40 MHz to 1 GHz frequency range using PAL D channel conditions.

1.4 Quick reference data

Table 1. Quick reference data

Bandwidth 40 MHz to 1003 MHz; V_B = 24 V (DC); $Z_S = Z_L$ = 75 Ω; T_{mb} = 35 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_p	power gain	f = 50 MHz		20.5	21.5	22.5	dB
		f = 1003 MHz		22	23	24	dB
CTB	composite triple beat	V_o = 48 dBmV at 862 MHz	[1][2]	-	−65	−59	dBc
CSO	composite second-order distortion	V_o = 48 dBmV at 862 MHz	[1][2]	-	−70	−60	dBc
I_{tot}	total current	pin 4 not connected	[3]	345	365	385	mA
		pin 4 connected to ground	[3]	-	315	-	mA

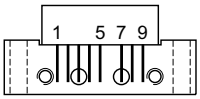
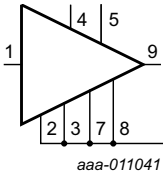
[1] 98 PAL D channels with 8 MHz bandwidth per channel; [f = 47 MHz to 862 MHz]; flat V_o till 862 MHz.

[2] Pin 4 not connected.

[3] Direct Current (DC).

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	input		
2, 3	common		
4	I_{CC} adjust [1]		
5	$+V_B$		
7, 8	common		
9	output		

[1] The total supply current can be adjusted by pin 4. Grounding of pin 4 gives the lowest supply current while floating of pin 4 gives the maximum supply current.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
CGD982LC	-	rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 × 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads	SOT115AE

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_B	supply voltage		-	30	V
$V_{i(RF)}$	RF input voltage	single tone	-	75	dBmV
I_I	input current	on I_{CC} adjust (pin 4)	–10	0	mA
T_{stg}	storage temperature		–40	+100	°C
T_{mb}	mounting base temperature		–20	+100	°C

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

5. Characteristics

Table 5. Characteristics

Bandwidth 40 MHz to 1003 MHz; V_B = 24 V (DC); $Z_S = Z_L$ = 75 Ω; T_{mb} = 35 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_p	power gain	f = 50 MHz		20.5	21.5	22.5	dB
		f = 1003 MHz		22	23	24	dB
SL_{sl}	slope straight line	f = 40 MHz to 1003 MHz	[1]	0.5	-	2	dB
FL	flatness of frequency response	f = 40 MHz to 1003 MHz	[2]	-	-	0.8	dB
RL_{in}	input return loss	f = 40 MHz to 160 MHz		20	-	-	dB
		f = 160 MHz to 320 MHz		20	-	-	dB
		f = 320 MHz to 640 MHz		19	-	-	dB
		f = 640 MHz to 870 MHz		17	-	-	dB
		f = 870 MHz to 1003 MHz		15	-	-	dB
RL_{out}	output return loss	f = 40 MHz to 160 MHz		20	-	-	dB
		f = 160 MHz to 320 MHz		20	-	-	dB
		f = 320 MHz to 640 MHz		19	-	-	dB
		f = 640 MHz to 870 MHz		17	-	-	dB
		f = 870 MHz to 1003 MHz		16	-	-	dB
NF	noise figure	f = 50 MHz		-	5.2	6.0	dB
		f = 1003 MHz		-	5.7	6.5	dB
Pin 4 not connected							
I_{tot}	total current		[3]	345	365	385	mA
98 PAL D channels							
CTB	composite triple beat	V_o = 48 dBmV at 862 MHz	[4]	-	–65	–59	dBc
CSO	composite second-order distortion	V_o = 48 dBmV at 862 MHz	[4]	-	–70	–60	dBc
Xmod	cross modulation	V_o = 48 dBmV at 862 MHz	[4][5]	-	–60	-	dB
59 PAL D channels + 75 digital channels							
CTB	composite triple beat	V_o = 58.5 dBmV at 1003 MHz	[6]	-	–72	-	dBc
CSO	composite second-order distortion	V_o = 58.5 dBmV at 1003 MHz	[6]	-	–75	-	dBc
Xmod	cross modulation	V_o = 58.5 dBmV at 1003 MHz	[5][6]	-	–67	-	dB
CCN	carrier-to-composite noise	V_o = 58.5 dBmV at 1003 MHz	[6]	-	62	-	dBc

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 5. Characteristics *...continued*

Bandwidth 40 MHz to 1003 MHz; V_B = 24 V (DC); $Z_S = Z_L$ = 75 Ω; T_{mb} = 35 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin 4 connected to ground							
I_{tot}	total current		[3]	-	315	-	mA
98 PAL D channels							
CTB	composite triple beat	V_o = 48 dBmV at 862 MHz	[4]	-	–58	-	dBc
CSO	composite second-order distortion	V_o = 48 dBmV at 862 MHz	[4]	-	–69	-	dBc
59 PAL D channels + 75 digital channels							
CTB	composite triple beat	V_o = 58.5 dBmV at 1003 MHz	[6]	-	–61	-	dBc
CSO	composite second-order distortion	V_o = 58.5 dBmV at 1003 MHz	[6]	-	–74	-	dBc
CCN	carrier-to-composite noise	V_o = 58.5 dBmV at 1003 MHz	[6]	-	55	-	dBc

[1] G_p at 1003 MHz minus G_p at 40 MHz.

[2] Flatness is defined as peak deviation to straight line.

[3] Direct Current (DC).

[4] 98 PAL D channels with 8 MHz bandwidth per channel; [f = 47 MHz to 862 MHz]; flat V_o till 862 MHz.

[5] Measured at 55.25 MHz.

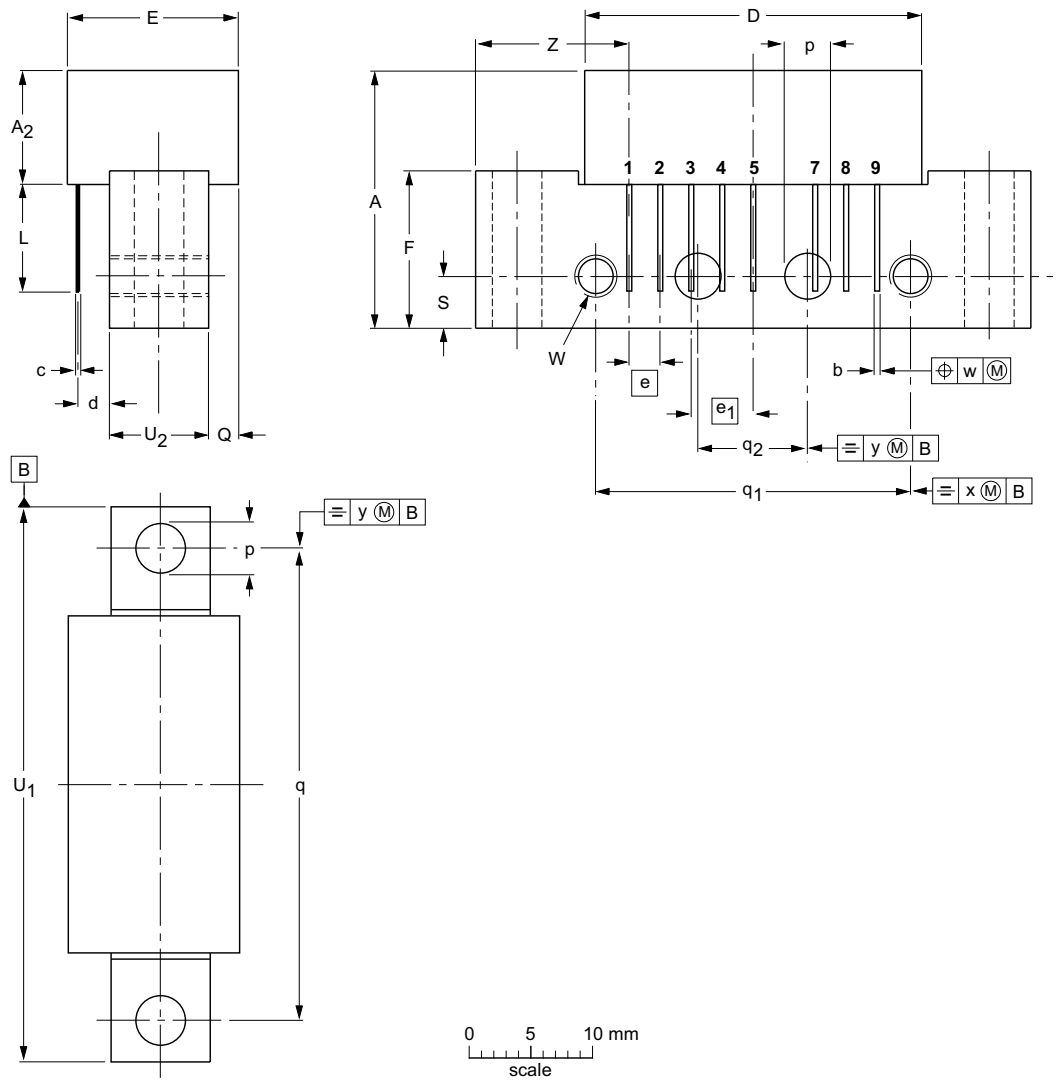
[6] 59 PAL D channels [f = 49.75 MHz to 543.25 MHz] + 75 digital channels [f = 555.25 MHz to 1003 MHz] (–10 dB offset); 13.5 dB tilt extrapolated to 1003 MHz.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6. Package outline

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads **SOT115AE**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	p	Q max.	q	q_1	q_2	S	U_1	U_2	W	w	x	y	Z max.
mm	20.8	9.5	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75 44.25	8.2 7.8	6-32 UNC	0.25	0.7	0.1	12

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT115AE						~~04-02-04~~ 10-06-18

Fig 1. Package outline SOT115AE

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7. Abbreviations

Table 6. Abbreviations

Acronym	Description
CATV	Community Antenna TeleVision
ESD	ElectroStatic Discharge
GaAs	Gallium-Arsenide
PAL D	Phase Alternate Line standard D
UNC	UNified Coarse

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CGD982LC v.1	20140310	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

9.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

10. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2 Pinning information 2
3 Ordering information 2
4 Limiting values 2
5 Characteristics 3
6 Package outline 5
7 Abbreviations 6
8 Revision history 6
9 Legal information 7
9.1 Data sheet status 7
9.2 Definitions 7
9.3 Disclaimers 7
9.4 Trademarks 8
10 Contact information 8
11 Contents 9

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 March 2014
Document identifier: CGD982LC